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**APPLICATION
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LETTERS PATENT**

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**FOR: METHOD FOR FABRICATING A
SEMICONDUCTOR DEVICE HAVING A
TAPERED-MESA SIDE-WALL FILM**

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METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE HAVING A TAPERED-MESA SIDE-WALL FILM

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BACKGROUND OF THE INVENTION

(a) Field of the Invention

10 The present invention relates to a method for fabricating a semiconductor device having a tapered-mesa side-wall film, and more particularly, to an improvement of the structure of an interlayer dielectric film embedding therein an interconnection layer.

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(b) Description of the Related Art

20 A multi-layer interconnection structure is generally employed in conventional semiconductor devices, such as a DRAM, for reducing the occupied area of the semiconductor devices. The multi-layer interconnection structure increases the integration density of the semiconductor device in association with the fine fabrication processes. The resultant semiconductor devices having a higher integration density generally have a higher aspect ratio and a smaller distance between each adjacent 25 two of the interconnects due to the smaller dimensions of the

devices in the horizontal directions.

Figs. 3A to 3E show consecutive fabrication steps of a process for fabricating a conventional multi-layer interconnection structure by using a two-layer hard mask. A metallic conductive layer 11a is first deposited on an underlying silicon oxide film 10, followed by deposition of the two-layer hard mask including an insulator film 12 and a silicon oxide film (oxide film) 13 consecutively as viewed from the bottom. The insulator film 12 may be a silicon nitride film (nitride film) having a sufficient etch selectivity relative to the oxide film 13. A photoresist film is then formed on the oxide film 13 by coating, followed by patterning thereof to obtain a photoresist pattern 14. The insulator film 12 and oxide film 13 are then etched by using the photoresist pattern 14 as a mask, to obtain the structure of Fig. 3A.

Subsequently, the photoresist pattern 14 is removed, followed by etching the metallic conductive film 11a to configure bit lines 11 having a specified width by using the insulator film 12 and oxide film 13 as a mask, as shown in Fig. 3B. Thereafter, as shown in Fig. 3C, another insulator film 15 is deposited on the entire surface, followed by etch-back thereof to configure side-wall films 16 on the bit lines 11a and corresponding insulator films 12, as shown in Fig. 3D. After this etching step, a portion of the oxide film 13 may be left on the insulator film 12, as illustrated by the dotted line in Fig. 3D.

After forming the side-wall film 16, an interlayer dielectric

film 17 is deposited to entirely embed therein the bit lines 11, insulator films 12 and side-wall films 16, as shown in Fig. 3E. It is to be noted that a defect, or void, is formed in the interlayer dielectric film 17 between side-wall films 16 (or bit lines 11).
5 The void is likely to occur in the case of a smaller distance between the bit lines 11 and the case of a higher aspect ratio of the insulator films 12 and side-wall films 16. In other words, a defective embedding structure of the interlayer dielectric film 17 may occur in the case of a smaller distance between the adjacent
10 side-wall films 16 and a larger depth of the side-wall films 16.

The two-layer hard mask may be replaced by a single-layer hard mask for patterning the bit lines 11. Figs. 4A to 4F show consecutive fabrication steps of another process using the single-layer hard mask in another conventional technique.

15 A metallic conductive film 11a and an insulator film 12 are consecutively formed on an underlying oxide film 10. Thereafter, a photoresist film is formed on the insulator film 12 by coating, followed by patterning thereof to form a photoresist pattern 14. By using the photoresist pattern as an etching mask, the insulator
20 film 12 is etched, as shown in Fig. 4A. After removing the photoresist pattern 14, the metallic conductive film 11a is then patterned using the insulator film 12 as a mask to configure bit lines 11 having a specified width just under the insulator film 12, as shown in Fig. 4B. An insulator film 15 is then deposited on the
25 entire surface, as shown in Fig. 4C, followed by etch-back thereof

to configure side-wall films 16 on both sides of the bit line 11 and the insulator film 12, as shown in Fig. 4D.

After the etch-back step, the insulator film 12 on the bit line 11 has a reduced thickness compared to the case using the two-layer hard mask, as illustrated by the dotted line in Fig. 4D. Subsequently, an interlayer dielectric film 17 is deposited to embed therein the insulator films 12 and the side-wall films 16, as shown in Fig. 4E. In this case using the single-layer hard mask, since the space between adjacent side-wall films 16 has a smaller depth, the defective embedding structure of the interlayer dielectric film such as encountered in the case of the two-layer hard mask is less involved in this case.

After forming the interlayer dielectric film 17, the interlayer dielectric film 17 is etched while using the insulator film 12 and the side-wall films 16 as an etch stopper in an self-alignment etching technique in order to form a contact hole for receiving therein a contact, i.e., self-aligned contact, for a capacitor between the bit lines 11. In this case of the single-layer hard mask, there may arise a problem that a short-circuit failure occurs between the self-aligned contact and one of the bit lines 11, as illustrated in Fig. 4F, due to the insufficient thickness of the insulator film 12 which may cause an exposed surface of the bit lines 11 during after self-alignment etching.

It is to be noted that a defective embedding structure of the interlayer dielectric film is more likely to occur along with the

development of the finer patterning process to reduce the space between adjacent interconnect lines. As described above, the two-layer hard mask causes the defective embedding structure due to the increased aspect ratio, wherein the space between the adjacent 5 side-wall films has a larger depth. On the other hand, the single-layer hard mask may cause a short-circuit failure due to reduction of the thickness of the insulator film and thus reduction of the etching margin during etching for the contact hole receiving therein the self-aligned contact, although there is some 10 improvement in the embedding structure itself.

Patent Publication JP-A-2000-31277 describes an improvement in the embedding structure formed by using the single-layer hard mask, wherein the embedding interlayer dielectric film is formed after removing the top corners of the 15 insulator film on an aluminum interconnect line. The described technique can reduce the effective aspect ratio by increasing the space between the adjacent insulator films in the vicinity of the top thereof due to the removal of the top corners of the dielectric film. However, this technique does not solve the above problem 20 of the short-circuit failure because the reduced thickness of the insulator film reduces the etch margin during etching for the self-aligned contact hole.

SUMMARY OF THE INVENTION

25 In view of the above problems in the conventional

techniques, it is an object of the present invention to provide a method for fabricating a semiconductor device having an improved embedding structure of the interlayer dielectric film and preventing the short-circuit failure after forming a contact 5 between interconnect lines, while using a two-layer hard mask for patterning the interconnect lines.

The present invention provides, in one aspect thereof, a method for fabricating a semiconductor device including the consecutive steps of: depositing a metallic conductive film on an 10 underlying insulating film; consecutively depositing first and second insulator films on the metallic conductive film; patterning the first and second insulator films to have a substantially same patterned area; etching the second insulator film selectively from the first insulator film to configure the second insulator film to 15 have a width smaller than a width of the first insulator film; patterning the metallic conductive film by using the first and second insulator films; depositing a third insulator film on the first and second insulator films and the underlying insulating film; etching-back the third insulator film to configure a side-wall film 20 covering at least the patterned metallic oxide film; and depositing a fourth insulator film over an entire area to embed therein the side-wall oxide film.

In accordance with the method of the present invention, since the side-wall film has a tapered mesa structure wherein the 25 top portion of the side-wall film has a smaller width compared to

the bottom portion thereof, the aspect ratio of the space between the side-wall films of the adjacent interconnect lines can be reduced for deposition of the fourth insulator films, whereby a defect of void can be prevented in the fourth insulator film
5 without decreasing the thickness of the first insulator film. The structure of the semiconductor device fabricated by the present invention is suited to a semiconductor memory device having a capacitor contact hole, which is formed in self-alignment etching process using the first insulator film and the side-wall film as an
10 etch stopper.

The above and other objects, features and advantages of the present invention will be more apparent from the following description, referring to the accompanying drawings.

15 BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1G are sectional views of a semiconductor device during consecutive steps of a fabrication process thereof according to a first embodiment of the present invention.

Figs. 2A to 2G are sectional views of a semiconductor device during consecutive steps of a fabrication process thereof according to a second embodiment of the present invention.

Figs. 3A to 3E are sectional views of a semiconductor device during consecutive steps of a conventional fabrication process therefor.

25 Figs. 4A to 4F are sectional views of a semiconductor

device during consecutive steps of another conventional fabrication process therefor.

PREFERRED EMBODIMENTS OF THE INVENTION

Now, the present invention is more specifically described with reference to accompanying drawings, wherein similar constituent elements are designated by similar reference numerals throughout the drawings for a better understanding of the present invention.

Referring to Figs. 1A to 1G, there is shown a method for fabricating a semiconductor device according to a first embodiment of the present invention. Roughly, the method of the present embodiment uses a two-layer hard mask for patterning bit lines, and deposits an interlayer dielectric film after protecting the patterned bit lines by using a side-wall oxide film having a tapered mesa structure.

A metallic conductive film 11a is first formed on an underlying oxide film 10, followed by forming thereon a two-layer hard mask including an insulator film 12 and an oxide film 13 consecutively as viewed from the bottom. The metallic conductive film 11a may include tungsten. A photoresist film is formed on the oxide film 13 by coating, followed by patterning the photoresist film to form a photoresist pattern 14. By using the photoresist pattern as a mask, the insulator film 12 and oxide film 13 are patterned by etching, as shown in Fig. 1A, to have a

substantially same patterned area. The insulator film 12 may be a nitride film, for example, which has a sufficient etch selectivity relative to the oxide film 13.

Thereafter, the photoresist pattern 14 is removed, followed
5 by wet etching the oxide film 13 in a desired amount by using an etchant such as diluted hydrofluoric acid (DHF) or buffered hydrofluoric acid (BHF), as shown in Fig. 1B. After this step, the resultant oxide film 13 has a smaller patterned area, i.e., smaller width, than the insulator film 12. Thereafter, the metallic
10 conductive film 11a is patterned by etching using the oxide film 13 and the insulator film 12 as an etching mask, to configure bit lines 11 each having a specified width equal to the width of the insulator film 12, as shown in Fig. 1C.

Subsequently, another insulator film 15 is deposited on the
15 entire surface, as shown in Fig. 1D, including the oxide film 13, insulator film 12, bit lines 11 and the underlying oxide film 10. The portion of the resultant insulator film 15 covering the oxide film 13, insulator film 12 and bit line 11 has a tapered mesa structure, wherein the insulator film has a larger width in the
20 vicinity of the underlying oxide film 10 than in the vicinity of the oxide film 13. The shape of the tapered mesa structure can be adjusted by selecting the thickness of the oxide film 13, the etching time for wet etching of the oxide film 13 etc.

The etch-back of the deposited insulator film 15 provides a
25 side-wall film 16 covering the side surfaces of the insulator film

12 and the bit line 11, as shown in Fig. 1E. At this step, a portion
of the oxide film 13 may be left on the insulator film 12.
Thereafter, an interlayer dielectric film 17 is deposited as by
using a high-density-plasma-enhanced CVD technique to embed
5 therein the insulator film 12 and the side-wall film 16, as shown
in Fig. 1F. Further, a contact hole 18 is formed between adjacent
bit lines 11 by etching the interlayer dielectric film 17 and the
underlying oxide film 10, while using a self-alignment etching
technique wherein the insulator film 12 and the side-wall film 17
10 are used as an etch stopper, the contact hole 18 receiving therein a
capacitor contact, as shown in Fig. 2G.

In the present embodiment, as described above, the bit line
11 is patterned using a two-layer hard mask including the
insulator film 12 and the oxide film 13 as an etching mask. After
15 the etch-back of the oxide film 13 selectively from the insulator
film 12, the insulator film 15 is deposited on the entire surface
and etched-back to form a side-wall film 16 for the bit line 11. In
such a configuration, since a sufficient thickness is secured for the
thickness of the insulator film 12 on the bit line 11 due to the use
20 of the two-layer hard mask, a short-circuit failure scarcely occurs
between each of the bit lines 11 and the capacitor contact formed
after the etching for the self aligned contact hole.

In addition, since the side-wall film 16 has a tapered mesa
structure, the top portion of the contract hole in the interlayer
25 dielectric film 17 is larger compared to bottom portion thereof in

the vicinity of the bit lines 11, a defective embedding structure can be suppressed in the deposition of the interlayer dielectric film 17 to prevent a "pair bit failure" in a semiconductor memory device. The pair bit failure often encountered in a conventional 5 semiconductor memory device is such that a pair of bit lines used for a column of memory cells and having a smaller space therebetween suffers from a defect of a short-circuit failure due to the contact disposed between the pair of bit lines.

Referring to Figs. 2A to 2G, there is shown a method for 10 fabricating a semiconductor device according to a second embodiment of the present invention. The second embodiment is similar to the first embodiment except that the oxide film 13 is etched after patterning the bit lines 11 in the second embodiment.

More specifically, metallic conductive film 11a, insulator 15 film 12 and oxide film 13 are consecutively deposited on an underlying oxide film 10. A photoresist film is then formed on the oxide film 13 by coating, followed by patterning thereof to form a photoresist pattern 14. Subsequently, the insulator film 12 and oxide film 13 are patterned by etching while using the 20 photoresist pattern as a mask, thereby configuring the insulator film 12 and oxide film 13 to have a substantially same patterned area, as shown in Fig. 2A.

Thereafter, the photoresist pattern 14 is removed, and the metallic conductive film 11a is patterned by etching, using the 25 oxide film 13 and insulator film 12 as a mask, to thereby

configure bit lines 11 having a specified width. Wet etching is then conducted to etch the oxide film 13 in a specified amount, as shown in Fig. 1C, wherein the oxide film 13 has a reduced patterned area compared to the insulator film 12. In other words,
5 the oxide film 13 has a smaller width than the insulator film 12. In addition, a surface portion of the underlying oxide film 10 is also removed by the wet etching. An insulator film 15 is then deposited over the entire surface as shown in Fig. 2D. The portion of the insulator film 15 covering the bit line 11 has a
10 tapered mesa structure, wherein the insulator film 15 has a smaller width in the vicinity of the oxide film 13 than in the vicinity of the underlying oxide film 10.

The insulator film 15 thus deposited is then etched-back to configure a side-wall oxide film 16, as shown in Fig. 2E. In the
15 etch-back step, a portion of the oxide film 13 may be left on the insulator film 12. Subsequently, an interlayer dielectric film 17 is deposited over the entire area to embed therein the insulator film 12 and side-wall oxide film 16, as shown in Fig. 2F. A self-alignment etching step is then conducted to form a self-aligned
20 contact hole 18 in the interlayer dielectric film 17 and the underlying oxide film 10 between the bit lines 12, as shown in Fig. 2G, followed by filling the contact hole 18 to form a capacitor contact.

In the present embodiment, although the surface portion of
25 the underlying oxide film 10 is removed during the selecting

etching of the oxide film 13, there are advantages that a larger etching margin is obtained during the self-alignment etching step for forming the contact hole 18 which is to receive therein the capacitor contact and that the interlayer dielectric film 17 less 5 suffers from a defective embedding structure compared to the conventional technique.

Since the above embodiments are described only for examples, the present invention is not limited to the above embodiments and various modifications or alterations can be 10 easily made therefrom by those skilled in the art without departing from the scope of the present invention. For example, the wet etching for the oxide film 13 as used in the step of Fig. 1B may be replaced by a dry etching, such as a sputter etching using argon gas, for reducing the width of the oxide film 13.